CLAIMS

What is claimed is:

1. A method of reducing distortion in a current steering DAC having a plurality of current steering switches, each current steering switch having first and second transistors with a common node coupled to a first current source, the method comprising, for each current steering switch:

providing a replica of the current steering switch, the replica switch having third and fourth transistors with a common node coupled to a second current source;

sensing the voltage variation on the common node of the replica of the current steering switch;

injecting charge onto the common node of the current steering switch responsive to the voltage variation on the common node on the replica of the current steering switch.

2. The method of claim 1 wherein the charge injected onto the common node of the current steering switch is proportional to the voltage variation on the common node on the replica of the current steering switch.

3. The method of claim 2 wherein the charge is injected by amplifying the voltage variation on the common

node on the replica of the current steering switch, and coupling the amplified voltage variation to the common node of the current steering switch through a coupling capacitor.

4. The method of claim 3 wherein the voltage variation on the common node on the replica of the current steering switch is amplified by a gain approximately equal to $(C_S + C_C)/C_C$, where C_S is the capacitance associated with the common node of the current steering switch and C_C is the capacitance of the coupling capacitor.

5. The method of claim 1 wherein the charge injected onto the common node of the current steering switch is approximately equal to the charge needed to change the voltage on a capacitance associated with the common node of the current steering switch by an amount equal to the change in voltage of an output of the current steering switch divided by the intrinsic gain of the switch transistor.

6. The method of claim 1 wherein each of the first and second transistors is terminated in a respective DAC load, and the third and fourth transistors are each terminated in a respective replica switch load.

7. The method of claim 1 wherein each of the first and second transistors is terminated in a respective DAC load,

and the third and fourth transistors are each also terminated in a respective one of the DAC loads.

8. The method of claim 7 wherein the ratio of the size of the first and second transistors to the size of the third and fourth transistors is n, where n is larger than 1, and the ratio of the first current source to the second current source is also n.

9. The method of claim 8 wherein the first and second current sources comprise a current splitter.

10. The method of claim 1 wherein the ratio of the size of the first and second transistors to the size of the third and fourth transistors is n, where n is larger than 1, and the ratio of the first current source to the second current source is also n.

11. The method of claim 10 wherein the first and second current sources comprise a current splitter.

12. The method of claim 1 wherein the current steering switch and the replica switch comprise transistor switches selected from the group consisting of MOS transistors, MESFET transistors, HEMT transistors, JFET transistors and bipolar junction transistors.

13. The method of claim 1 wherein the current steering switch and the replica switch are CMOS switches, and wherein the body of each CMOS switch is connected to its source.

14. The method of claim 1 wherein the current steering switch and the replica switch are CMOS switches, and wherein the body of each CMOS switch is connected to a voltage other than its source.

15. A method of reducing third harmonic distortion in a current steering DAC having a plurality of current steering switches, each current steering switch having first and second transistors with a common node, each of the first and second transistors being terminated in a respective DAC load, the method comprising, for each current steering switch:

splitting a steering current to provide first and second current sources, the first current source being coupled to the common node of the first and second transistors, the first current source being n times the second current source, wherein n is larger than 1;

providing a replica of the current steering switch, the replica switch having third and fourth transistors with a common node coupled to the second current source, each of the third and fourth transistors also being terminated in a respective DAC load, each of the third and fourth transistors

being switched in unison with a respective one of the first and second transistors, the first and second transistors being larger than the third and fourth transistors by the factor n;

sensing the voltage variation on the common node of the replica of the current steering switch;

injecting charge onto the common node of the current steering switch responsive to the voltage variation on the common node on the replica of the current steering switch.

16. The method of claim 15 wherein the charge injected onto the common node of the current steering switch is proportional to the voltage variation on the common node on the replica of the current steering switch.

17. The method of claim 16 wherein the charge is injected by amplifying the voltage variation on the common node on the replica of the current steering switch, and coupling the amplified voltage variation to the common node of the current steering switch through a coupling capacitor.

18. The method of claim 17 wherein the voltage variation on the common node on the replica of the current steering switch is amplified by a gain approximately equal to $(C_S + C_C)/C_C$, where C_S is the capacitance associated with the

common node of the current steering switch and C_C is the capacitance of the coupling capacitor.

19. The method of claim 15 wherein the charge injected onto the common node of the current steering switch is approximately equal to the charge needed to change the voltage on a capacitance associated with the common node of the current steering switch by an amount equal to the change in voltage of an output of the current steering switch divided by the intrinsic gain of the switch transistor.

20. The method of claim 15 wherein the current steering switches and the replica switches comprise transistor switches selected from the group consisting of MOS transistors, MESFET transistors, HEMT transistors, JFET transistors and bipolar junction transistors.

21. The method of claim 15 wherein the current steering switches and the replica switches are CMOS switches, and wherein the body of each CMOS switch is connected to its source.

22. The method of claim 15 wherein the current steering switches and the replica switches are CMOS switches, and wherein the body of each CMOS switch is connected to a voltage other than its source.

23. A current steering DAC comprising a plurality of controllable current sources, each current source comprising:

a first current switch having first and second transistors with a common node coupled to a first current source, the transistors each being coupled to a respective one of first and second DAC loads and each having a control terminal for steering the current of the first current source to the first or the second DAC load responsive to a differential signal applied to the control terminals of the first and second transistors;

a second current switch having third and fourth transistors with a common node coupled to a second current source, the third and fourth transistors each being coupled to a respective one of the first and second DAC loads and each having a control terminal for steering the current of the second current source to the first or the second DAC load responsive to the differential signal as also applied to the control terminals of the third and fourth transistors; and,

a charge injection circuit injecting a charge into the common node of the first and second transistors responsive to the change in voltage of the common node of the third and fourth transistors.

24. The current steering DAC of claim 23 wherein the charge injection circuit is a circuit for injecting a charge

proportional to the voltage variation on the common node of the third and fourth transistors.

25. The current steering DAC of claim 24 wherein the injection circuit is comprised of an amplifier coupled to amplify the voltage change on the common node of the third and fourth transistors and a capacitance coupled between an output of the amplifier and the common node of the first and second transistors.

26. The current steering DAC of claim 25 wherein the capacitance and the gain of the amplifier are selected so that the gain of the amplifier is approximately equal to $(C_S + C_C)/C_C$, where C_S is the capacitance associated with the common node of the first and second transistors and C_C is the capacitance of the coupling capacitor.

27. The current steering DAC of claim 23 wherein the first, second, third and fourth transistors comprise a type of transistor selected from the group consisting of MOS transistors, MESFET transistors, HEMT transistors, JFET transistors and bipolar junction transistors.

28. The current steering DAC of claim 23 wherein the first, second, third and fourth transistors are CMOS

transistors having a source, drain and gate, and wherein the body of each CMOS transistor is connected to its source.

29. The current steering DAC of claim 23 wherein the first, second, third and fourth transistors are CMOS transistors having a source, drain and gate, and wherein the body of each CMOS transistor is connected to a voltage other than its source.